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18CS33

Third Semester B.E. Degree Examination, July/August 2022
Analog and Digital Electronics

Time: 3 hrs.   Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the working principal of photodiode and discuss its applications. **(08 Marks)**
  b. Design a monostable multivibrator circuit using 555 Timer IC to generate an output pulse of 100 ms. Choose C = 0.47 µF. Draw the circuit. **(06 Marks)**
  c. Give the typical application of A/D and D/A converters with a block diagram. **(06 Marks)**

OR

2 a. Obtain the expression for collector to emitter voltage for voltage divider bias of BJT using accurate analysis. **(08 Marks)**
  b. Design and draw astable multivibrator circuit using 555 Timer IC to generate 1 kHz square wave (Duty cycle = 50 %). Assume C = 0.1 µF. **(06 Marks)**
  c. Explain R-2R ladder type DAC with a neat diagram. **(06 Marks)**

Module-2

3 a. Define prime implicant and essential prime implicant. Give an example. **(04 Marks)**
  b. Use a Karnaugh map to find the minimum sum-of-products form for,
     $$F(A,B,C,D) = \sum m(0,2,4,10,11,14,15) + \sum d(6,7)$$ **(06 Marks)**
  c. Find a minimum sum-of-products solution using the Quine-McClusky method for given function,
     $$f(w,x,y,z) = \sum m(1,3,6,7,8,9,10,12,13,14)$$ **(10 Marks)**

OR

4 a. Obtain the minimum product of sums for $f(w,x,y,z) = \bar{x}\,\bar{z} + wyz + \bar{w}\,\bar{y}\,\bar{z} + x\bar{y}$ using Karnaugh map. **(08 Marks)**
  b. Find all prime implicants of the given function $F = \sum m(0,1,2,5,6,7)$, and find all minimal solutions using Petrick's method. **(08 Marks)**
  c. Explain simplification of logic functions using map-entered variables. **(04 Marks)**

Module-3

5 a. Realize the given function $f = \bar{b}\,\bar{c} + a\bar{b} + \bar{a}b$ using only two-input NAND gates. **(06 Marks)**
  b. Discuss different types of hazards in combinational logic circuits. **(06 Marks)**
  c. What is Programmable Array Logic (PAL)? Show the implementation of a full adder using a PAL. **(08 Marks)**

OR

6 a. What is a multiplexer? Write the logic diagram for 8 : 1 multiplexer using 4 input AND and OR gates. **(08 Marks)**
  b. Discuss the four kinds of three state buffers. **(08 Marks)**
  c. Explain programmable logic array structure. **(04 Marks)**

Module-4

7   a.   What is VHDL? Show how to model the 4-to-1 multiplexer using a VHDL conditional assignment statement. **(06 Marks)**

    b.   Derive the characteristic equation for S-R flip-flop and J-K flip-flop in product-of-sums form. **(06 Marks)**

    c.   What is D flip-flop? Illustrate the operation of the clear and preset inputs in D-flip-flop with timing diagram. **(08 Marks)**

OR

8   a.   Show how to construct a VHDL module using an entity architecture pair. **(06 Marks)**

    b.   Explain switch debouncing with an S-R latch. **(06 Marks)**

    c.   What is T flip-flop? Show how to convert D-flip-flop into T-flip-flop. **(08 Marks)**

Module-5

9   a.   What is a register? Build a parallel adder with an accumulator using registers. **(06 Marks)**

    b.   Design 3-bit synchronous counter using T-flip-flops. **(08 Marks)**

    c.   Design a sequential parity checker for serial data. **(06 Marks)**

OR

10 a.   Explain the working of a 3 bit shift register. **(06 Marks)**

    b.   Distinguish ring counter and Johnson counter. Also give the general form of a shift register counter. **(06 Marks)**

    c.   Design 3-bit binary synchronous down counter using J-K flip-flops. **(08 Marks)**

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